IN THE SPECIFICATION:

Please replace paragraph number **[0003]** with the following rewritten paragraph:

[0003] One approach for improving packaging density of integrated circuits has been to place chips on a circuit board in a vertically stacked arrangement. In such approaches, chips are generally packaged and then the individual packages are stacked in a vertical arrangement. Vertical ~~packages~~ package approaches have utilized an intricate and sophisticated cross-wiring approach which modifies the individual chips so that they may be stacked by adding a pattern of metallization, often called rerouting leads, to the surface of the wafer. Such rerouting leads extend from the bond pads of the chip to newly formed bond pads that may be arranged along the terminating edge of the chip. In such a configuration, each modified chip is then cut from the wafer and assembled into a stack such that all of the leads of the modified chips are aligned along the same side of the stack resulting in a vertical interconnection of the individual chips. Such approaches result in only modest volumetric improvements at a great interconnection expense that presents many opportunities for failure as well as ~~requiring~~ requires intricate assembly approaches.

Please replace paragraph number **[0004]** with the following rewritten paragraph:

[0004] Other approaches for arraying or otherwise assembling multiple integrated circuits in a more volume-efficient approach include the formation of memory modules which are formed from individual dice that are assembled individually on a common printed circuit board with each of the pads from an individual die routed to the external printed circuit board which provides the interconnection to an adjacent die or dice. While such an approach reduces the number of packages per die, as a plurality of dice are placed on a single printed circuit board and then packaged into a larger memory module assembly, such an approach still results in significant spacing between each of the individual ~~die~~ dice in order to accommodate manufacturing processes for externally coupling die pads from one integrated circuit to adjacent integrated circuits. Therefore, there is a need for providing an improved and volumetrically more

efficient coupling of integrated circuit chips without incurring significant expense of assembling and interconnecting multiple ~~die~~ dice for use in a higher assembly package.

Please replace paragraph number **[0005]** with the following rewritten paragraph:

[0005] A semiconductor wafer having a plurality of dice thereon is manufactured using conventional processing techniques. The wafer is subjected to probe testing or other testing to identify functional and nonfunctional dice. The locations of the functional dice are analyzed to determine the presence of clusters of functional dice or at least the location of adjacent functional dice. A group of functional dice is identified and an interconnection circuit is formed for routing together the signals of adjacent ~~die~~ dice at the wafer-level to minimize external interconnections once the dice are segmented into devices. The functional die group, once interconnected, is then segmented from the wafer while maintaining the unitary structural integrity of the functional die group as well as the associated interconnections between dice. Wafer-level interconnection of functional dice reduces volumetric requirements on the next higher assembly as well as reduces interconnection labor and dimensions by maintaining die-to-die interconnection at the semiconductor wafer-level.

Please replace paragraph number **[0006]** with the following rewritten paragraph:

[0006] The present invention includes several approaches for forming the interconnection circuit including the identification of functional dice and the formation of the circuit specifically between the functional dice as well as an approach to form an interconnection circuit over entire portions of the semiconductor wafer with the nongrouped portions becoming electrically isolated when individual groups of dice become segmented. The interconnection circuit, in one embodiment, is formed using redistribution layer techniques for forming electrical contacts with bond pads of individual dice. The interconnection circuit includes conductive segments that are routed between respective bond pads of adjacent or nearly adjacent dice. Another embodiment of the present invention teaches coupling functional dice together that are separated from each other by one or more nonfunctional dice. In such an embodiment, the

interconnection circuit may also couple to the bond pad of a nonfunctional die which provides the bridging of electrical conductive segments between functional dice. Techniques are also disclosed for isolating the circuitry of the nonfunctional die to prevent undesirable capacitance or loading of the desired signal. A memory module as well as an electronic system interconnected with functional die groups is also encompassed by the present invention.

Please replace paragraph number **[0009]** with the following rewritten paragraph:

[0009] FIG. 2 is a detailed illustration of a semiconductor wafer having identified groups of functional ~~die~~ dice thereon, in accordance with an embodiment of the present invention;

Please replace paragraph number **[0010]** with the following rewritten paragraph:

[0010] FIG. 2A is a detailed view of one of the functional die groups ~~and~~ and an associated interconnection circuit, in accordance with an embodiment of the present invention;

Please replace paragraph number **[0012]** with the following rewritten paragraph:

[0012] FIG. 3 is a detailed view of a semiconductor wafer having groupings of functional ~~die~~ dice identified thereon;

Please replace paragraph number **[0013]** with the following rewritten paragraph:

[0013] FIG. 3A is a detailed view of an adjacent die interconnection circuit for coupling adjacent functional ~~die~~ dice within a group, in accordance with another embodiment of the present invention;

Please replace paragraph number **[0014]** with the following rewritten paragraph:

[0014] FIG. 4 is a view of a memory module for coupling thereon an integral plurality of functional ~~die~~ dice interconnected according to an embodiment of the present invention;

Please replace paragraph number **[0017]** with the following rewritten paragraph:

[0017] FIG. 5 is a view of a semiconductor wafer having identified groupings of functional ~~die~~ dice for interconnecting in accordance with an embodiment of the present invention;

Please replace paragraph number **[0018]** with the following rewritten paragraph:

[0018] FIG. 5A is a detailed view of an adjacent die interconnection circuit for coupling nearly adjacent groups of functional ~~die~~ dice, in accordance with an embodiment of the present invention;

Please replace paragraph number **[0030]** with the following rewritten paragraph:

[0030] The present invention contemplates the coupling of several functional dice together with the respective bond pads of each functional dice operably coupled together through an adjacent die interconnection circuit. Therefore, an adjacent die interconnection circuit that operably couples multiple dice includes a corresponding number of conductor segments that electrically link between a bond pad of one die to the bond pad of the adjacent die, etc. Therefore, by way of example, a semiconductor device comprised of three adjacent functional ~~die~~ dice would include an adjacent die interconnection circuit that is comprised of a first conductor segment for linking the first and second dice together and then a second conductor segment for linking the second and third dice together.

Please replace paragraph number **[0031]** with the following rewritten paragraph:

[0031] The adjacent die interconnection circuit 50 may be fabricated using photolithographic patterning of a deposited metal layer through the use of a single reticle for each type of functional die group (*e.g.,* two dice, three dice, four dice, etc.) which, in the present embodiment may be aligned with each functional die group for the formation of the adjacent die interconnection circuit 50. Such a reticle pattern may accommodate the formation of conductor segments and, additionally, may facilitate the formation of bumped contacts on one or more of

the adjacent functional ~~die~~ dice to form an interconnection pattern as illustrated in FIG. 2. The interconnection pattern illustrated in FIG. 2 couples together functional dice that have an adjacently functional counterpart for the formation of a functional die group.

Please replace paragraph number **[0032]** with the following rewritten paragraph:

[0032] FIG. 3 illustrates an alternative embodiment for the coupling of functional dice. In similar manner with the previous embodiment, the individual dice on wafer 60 undergo probe testing for the identification of functional and nonfunctional dice. The test results of the probe testing process are obtained and analyzed to identify adjacent functional dice for the formation of functional die groups. The identification of functional die groups, such as functional die groups ~~62-70~~ 62, 64, 68, 70, identifies functional dice candidates for forming into semiconductor devices, namely interconnected functional die groups. In the present embodiment, however, rather than coupling together only those functional dice which are aggregated into a functional die group, some nonfunctional ~~die~~ dice are also included within the formation of adjacent die interconnection circuits.

Please replace paragraph number **[0033]** with the following rewritten paragraph:

[0033] FIG. 3A illustrates the coupling of functional dice 72-78 through the formation of adjacent die interconnection segments ~~82-84~~ 80-84 for the coupling of their respective bond pads. Similarly, functional die groups 64 and 70 are also routed to adjacent functional ~~die~~ dice for the formation of the respective semiconductor devices, namely interconnected functional die groups. However, the present embodiment also contemplates formation of the adjacent die interconnection circuits between adjacent functional ~~die~~ dice by coupling at least some nonfunctional ~~die~~ dice together with adjacent functional ~~die~~ dice before segmentation. Such a process may be performed on a portion of the wafer or adjacent die interconnection circuits may be formed throughout an entire die with the coupling of functional ~~die~~ dice to nonfunctional die being severed during the segmentation process wherein functional and nonfunctional die are diced or segmented.

Please replace paragraph number **[0034]** with the following rewritten paragraph:

[0034] Referring to FIG. 4, a memory ~~module~~ module 90 in accordance with the present ~~invention,~~ invention is illustrated as having an elongate carrier substrate 92, such as a printed circuit board (PCB) or other substrate known in the art to which a plurality of functional ~~die~~ dice are attached. The plurality of functional dice are integral in form and are not individually segmented as in the case of prior art applications but comprise a single contiguous semiconductor substrate and are interconnected with one another according to the formation of the adjacent die interconnection circuits previously described. Coupling of the semiconductor device, illustrated as interconnected functional die group 94, with substrate 92, in one embodiment, may be accomplished through the use of flip-chip bonding wherein the plurality of functional chips are provided with conductive bumps, shown as conductive bumps 42 in FIG. 4A, with each conductive bump 42 electrically coupled to a functionally-like bond pad of each functional die within the interconnected functional die group 94. Interconnected functional die group 94 is operably coupled with substrate 92 by superimposing the conductive bumps 42 over similarly configured substrate contacts or terminal pads 96 on the surface of substrate 92, at which time the conductive bumps 42 (if solder) are heated and melted or "reflowed" to form mechanical and electrical connections between the substrate 92 and functional die group 94. Alternatively, the functional die group 94 may be wire bonded by wire bonds 102 to the substrate 92, as illustrated in FIG. 4B, by wire bonding from adjacent die interconnection segments (*e.g.,* segments 34-38 (FIG. 2A) and segments ~~82-84~~ 80-84 (FIG. 3A)) to substrate contacts 96 which further couple via conductors 98 to PCB electrical contacts 100. The use of TAB connections comprising conductive traces on flexible dielectrics, as well as the use of edge connects in a vertical surface mount configuration, are also contemplated.

Please replace paragraph number **[0035]** with the following rewritten paragraph:

[0035] In accordance with a further embodiment, the die group 94 of FIG. 4 may be interconnected one with another, either partially or in totality through ~~conduits~~ conductors 98 on

substrate 92. In the present embodiment, the ~~conduits~~ conductors 98 may provide electrical coupling between each of the, for example, conductive bumps 42 (FIG. 4A) rather than rely upon conductive traces formed on the die group 94.

Please replace paragraph number **[0036]** with the following rewritten paragraph:

[0036] FIGs. 5 and 5A illustrate another embodiment for coupling together relatively adjacent groups of functional ~~die~~ dice. In FIG. 5, a wafer 104 is illustrated as having two relatively adjacently located functional die groups 106 and 108 which are separated by a nonfunctional die 110. The present invention contemplates the coupling of relatively adjacent functional die groups, such as functional die groups 106 and 108 into a single semiconductor device, illustrated as interconnected functional die group 112.

Please replace paragraph number **[0037]** with the following rewritten paragraph:

[0037] FIG. 5A illustrates the coupling of functional die groups 106 and 108 via bridging nonfunctional die 110 through the use of an adjacent die interconnection circuit 50 described previously. In the present embodiment, the adjacent die interconnection segments 114 couple the functional ~~die~~ dice of functional die group 106 and adjacent die interconnection segments 116 couple the functional ~~die~~ dice within functional die group 108. Additionally, the present embodiment further utilizes adjacent die ~~interconnect~~ interconnection segments 118 and 120 for bridging an electrical interconnect across the nonfunctional die 110. Following the coupling together of functional die groups 106 and 108, the entire five-die assembly may then be unitarily segmented from the wafer as a semiconductor device, illustrated as interconnected functional die group 112.

Please replace paragraph number **[0038]** with the following rewritten paragraph:

[0038] FIGs. 6 and 7 contemplate the deleterious effects associated with having a nonfunctional die within a larger assembly, namely the undesirable aberrational behavior or at least the undesirable additional capacitance associated with unnecessary circuitry attached to

adjacent die interconnect segments. In FIG. 6, adjacent die ~~interconnect~~ interconnection segments 118 and 120 bridge the coupling of functional die groups 106 and 108 through the coupling of the respective bond pads 122 and 124. However, bond pad 126 of nonfunctional die 110 is isolated through the process of open circuiting a nonfunctional die bond pad isolation conductive segment 128 through a manufacturing process such as laser ablation or through the use of an etching process through foregoing ~~on~~ an interconnection processing step that generates an interconnect between bond pad 126 and conductive segment 128. Alternatively, FIG. 7 depicts the isolation of bond pad 126 from adjacent die ~~interconnect~~ interconnection segments 118 and 120 through the use of a gating or isolation device 130 which may be further controlled by an isolation control signal 132. Other forms of isolating bond pad 126 and the associated capacitance and deleterious effects associated therewith are also contemplated as within the scope of the present invention.

Please replace paragraph number **[0041]** with the following rewritten paragraph:

[0041] It will be appreciated by those skilled in the art that various circuits and methods can be used to achieve the desired memory capability of the memory module, through the incorporation of a varying number of functional dice which may be coupled to one another through the adjacent die interconnection circuit described herein, or may alternatively be coupled to other functional dice via adjacent nonfunctional die or dice. Those of ordinary skill in the art also ~~appreciated~~ appreciate that the number and configuration of the dice, as well as the geometric relationship with other neighboring devices, whether functional or nonfunctional, are also contemplated and the immediate adjacent nature of the functional and nonfunctional die as illustrated herein are but one example of relationships of a die with other dice on an integral wafer. Additionally, the bonding techniques for attaching and electrically interconnecting the semiconductor device (e.g., interconnected functional die group) with the substrate according to the methods described herein, are also but an example that is not to be considered limiting.